IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 5, line 5 is amended as follows:

Figure 1 is a block diagram of a communications transceiver 100 according to one embodiment of the present invention. The communications transceiver 100 includes a link level protocol (LLP) 110, a driver 130, a canceller/equalizer 120, and a receiver 140.

The paragraph beginning at page 5, line 24 is amended as follows:

The driver 130 includes a driver circuit 134 and an impedance controller 132. The impedance controller 132 connects to driver circuit 134 via an impedance controller line 136. The impedance controller 132 continuously monitors the impedance of the communication channel by monitoring signals representing voltage, temperature, or other variation or process characteristics of the communications medium. The impedance controller 132 then interacts with the driver circuit to automatically drive a signal through the driver output 138 with an output impedance matching that of the communication medium. For more specific details on how the impedance controller works, see "Impedance Controller" U.S. Patent No. 6,703,908, Issued, March 9, 2004 ~~U.S. Patent Application Serial No. (Attorney Docket # 499.073US1)~~, which is incorporated by reference.

The paragraph beginning at page 6, line 23, is amended as follows:

In one embodiment, receiver 140 receives the equalized signal from the canceller/equalizer output 121. The receiver includes a receiver circuit 142 connected to the canceller/equalizer output 121, a clock receiver 144 receiving a clock signal 145, and a bit deskew 146 connected to the receiver circuit line 143 and the receiver line 116. As described in "System and Method for Adaptively Deskewing Parallel Data Signals Relative to a Clock" U.S.

Patent Application Serial No. 09/476678, the description of which is incorporated herein by reference, the bit deskew 146 continuously tracks data and continuously corrects skew among data lines in the communications medium. The bit deskew 146 can coarse tune or fine tune the received signal with a potential for up to 3.75ns of deskew at an 800Mb per second signaling rate. The bit deskew ~~146can~~ 146 can also center the clock signal on the clock line 145 received by the clock receiver 144. Of course, these are only a few of the general capabilities of the bit deskew 146. For others, refer to "System and Method for Adaptively Deskewing Parallel Data Signals Relative to a Clock" U.S. Patent Application Serial No. 09/476678.

The paragraph beginning at page 8, line 16 is amended as follows:

The drivers and receivers of the present invention may transmit and receive data utilizing, what can be termed, Path Forward Source Synchronization. If so, driver 130, 230 or 330 may be called a ~~PathForward~~ Path Forward Source Synchronous Driver (PFSSD) and receiver 140, 240, or 340 may be called a ~~PathForward~~ Path Forward Source Synchronous Receiver (PFSSR). The sections below entitled "PFSSD" and "PFSSR" describe how to implement PFSSDs and PFSSRs into the embodiments of the present invention.

The paragraph beginning at page 22, line 14 is amended as follows:

Figure 12 shows a schematic of a simplified reference generator 1200. ~~Both a~~ Both "right-hand" and "left-hand" ~~generator~~ generators are shown for clarity. Each generator consists of a terminator 1210 matched to the transmission line 1215 and a canceller/equalizer 1220. The transmission line 1215 is indistinguishable from the lines used for data: of the same type, connected the same as data lines, and physically located with data lines. Thus, the common-mode noise signals at points L and R in the figure should closely match the common- mode noise signals on the left and right data lines. The terminators have nominal output voltages of $V_{dd}/2$, and their output resistances are set in the same manner as the transmitters described above. Thus, their characteristics match those of the data transmitters, and track variations with process, voltage, and temperature. The canceller/equalizers 1220 are hard wired so as to disable an

offsetting feature of the canceller/equalizer's 1220 (by connecting PREFT to V_{dd} and NREFT to ground), and to enable its output drive capability (CANEN to V_{dd}). Thus, the canceller/equalizer's 1120 outputs track their individual inputs. This tracking may not be exact: the canceller/equalizer 1220 has a non- unity gain and may have an offset. However, the effects of the canceller/equalizers 1220 in the common-mode reference module matches those of the canceller/equalizers in the data paths. The distributed reference signal 1225 is not offset from the common-mode voltage out of the canceller/equalizer 1220 in any data path by more than ± 20 mV in steady state. The 3-dB bandwidth of the reference generator is not less than 100 MHZ. The output resistance of the voltage buffer in the reference generator 1200 does not exceed 1 KΩ. One reference generator 1200 is provided for each data bus, with the reference voltage distributed to all receivers within the bus. The wire carrying the reference is isolated from parallel traces to reduce the coupling of noise onto the reference trace. This isolation consists of an empty area on either side of the reference trace. Specifically, the reference line is a 0.84 micron wire shielded on both sides by 0.28 micron wires, one connected to V_{dd} and the other connected to V_{ss}. Separation between the reference wire and shield wires is 0.28 micron. Maximum length of the reference net is 10 mm, and maximum resistance of the net from end to end is 10,000 microns x 0.09 ohms/micron = 900 ohms.